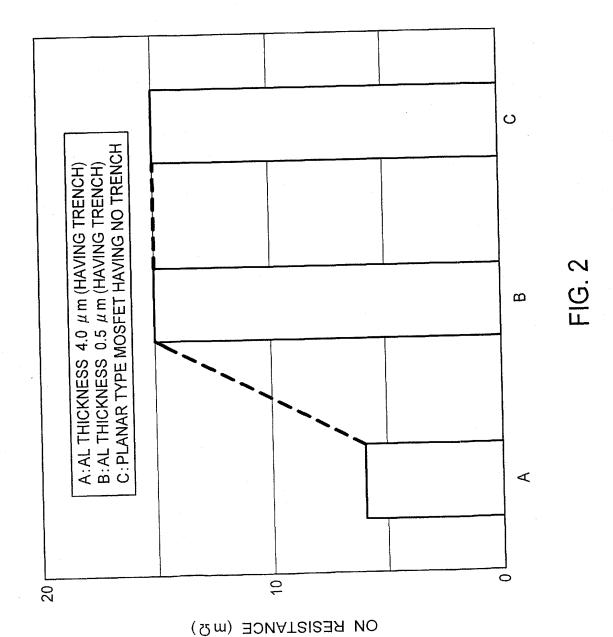


FIG. 1

The state of the s



2/9

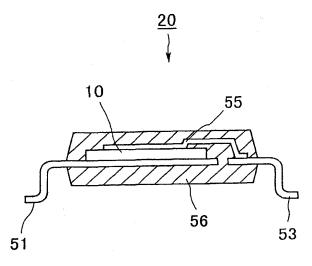


FIG. 3A

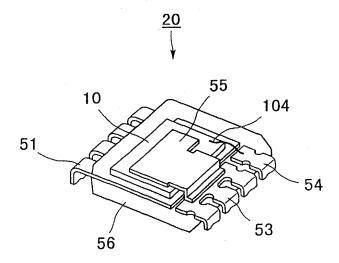
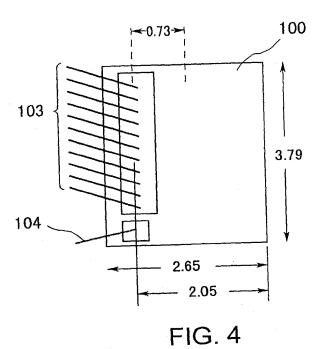


FIG. 3B

the state of the s



The state of the s

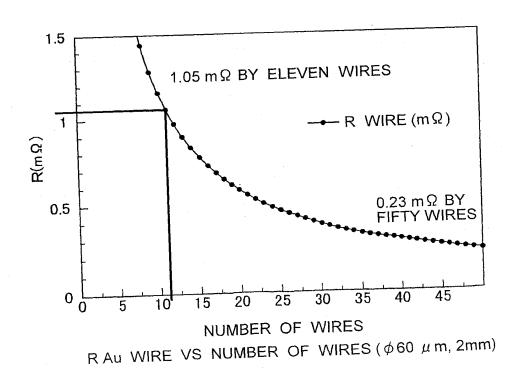
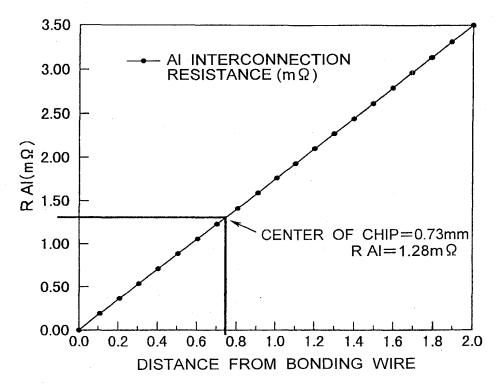


FIG. 5



AI INTERCONNECTION RESISTANCE ON SURFACE OF CHIP

FIG. 6





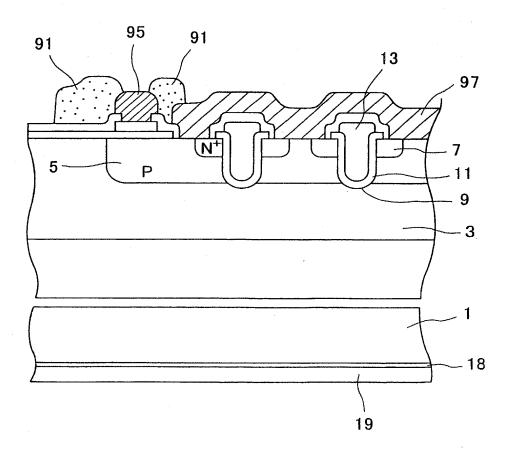


FIG. 7

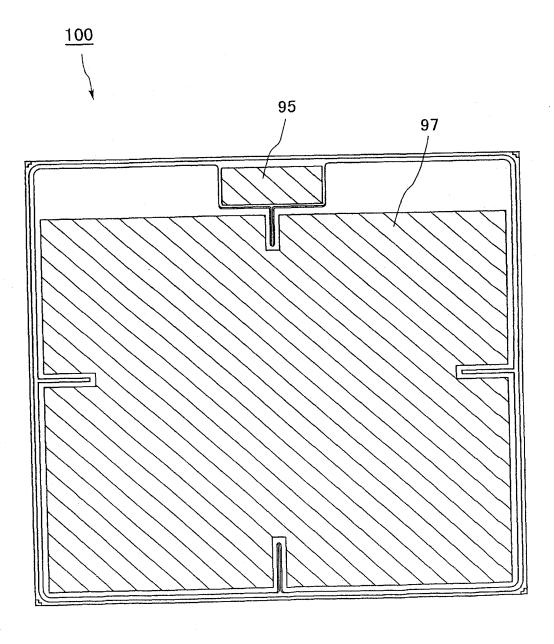


FIG. 8

And the state of t



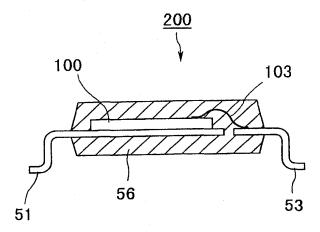


FIG. 9A

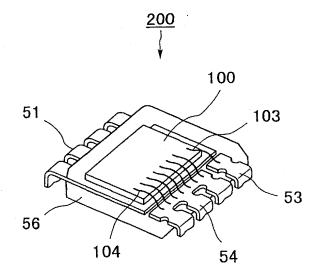


FIG. 9B

SERIAL NO: 10/020,928 INV: Shigeo KOUZUKI, et al. DOCKET # 217636US3 SHEET 9 OF 9



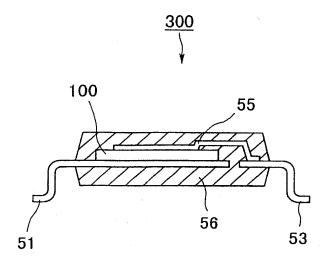


FIG. 10A

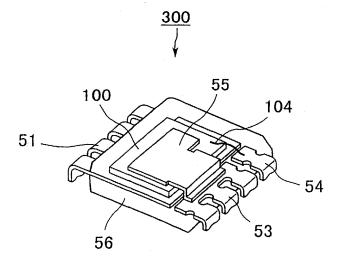


FIG. 10B